



# **BL-M8715QT4**

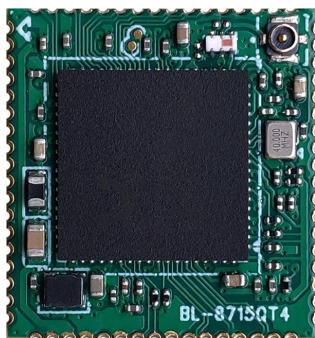
**802.11ac 150M 1T1R WLAN**

**Camera Module Specification**

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(Top View)



(Bottom View)

|                                                   |       |
|---------------------------------------------------|-------|
| Module Name: BL-M8715QT4                          |       |
| Module Type: 802.11b/g/n/ac 150Mbps Camera Module |       |
| Revision: V1.0                                    |       |
| Customer Approval:                                |       |
| Company:                                          |       |
| Title:                                            |       |
| Signature:                                        | Date: |
| BL-link Approval:                                 |       |
| Title:                                            |       |
| Signature:                                        | Date: |

## Revision History

| Revision | Summary                      | Release Date |
|----------|------------------------------|--------------|
| 0.1      | Initial release              | 2021-05-15   |
| 0.11     | Initial release(update spec) | 2021-06-19   |
| 1.0      | Official release             | 2023-01-09   |

## 1. Introduction

### 1.1 General description

The BL-M8715QT4 is a Highly integrated ultra-low power IP camera module base on RTL8715AQD, which combines ARM v8M CPU, Memory unit, Security unit, Power management unit, Video unit, Audio unit, WLAN unit in a single chip. It provides rich functional interfaces such as analog audio, MIPI video, USB 2.0 host or device, SDMMC HS or SDIO device, RMII, it also provides a bunch of configurable GPIOs which are configured as digital peripherals, ADC inputs, PWM outputs. With so many advantages, BL-M8715QT4 ideal for multi-function, small size and cost-effective high-definition IP cameras!

### 1.2 Features

#### **Video**

- Support MIPI CSI-2 two data lane interface CMOS sensor
- Integrated image signal processor supports multiple and professional image processing functions
- Support digital image stabilization(720p)
- Support motion detection and private mask
- Integrated Encoder supports Max 2megapixel resolution for H.264 encoding with multiple profiles and levels
- Support multiple stream real-time H.264/JPEG JPEG encoding outputs with individual scaling down size
- Support Constant Bit Rate/Variable Bit Rate control

#### **Audio**

- Integrated Audio Codec with 16 bit DAC and ADC, 5band configurable EQ supported
- Support Mono Speaker output with 16Ω and 32Ω loading
- Support Mono Microphone input with build-in Mic bias generator

#### **CPU and Memory**

- ARM v8M MCU with 300MHz clock and 2.23 DMIPS/MHz
- Embedded 32MB LPDDR1 memory up to 200MHz
- Support external (on customer's mainboard, 1.8V I/O ) SPI/QPI NOR Flash

#### **WLAN**

- Operating Frequencies: 2.4~2.4835&5.15~5.85GHz
- Compatible IEEE 802.11b/g/n/ac 1T1R WLAN PHY rate up to 150Mbps

- Connect to the external antenna through IPEX-4 connector

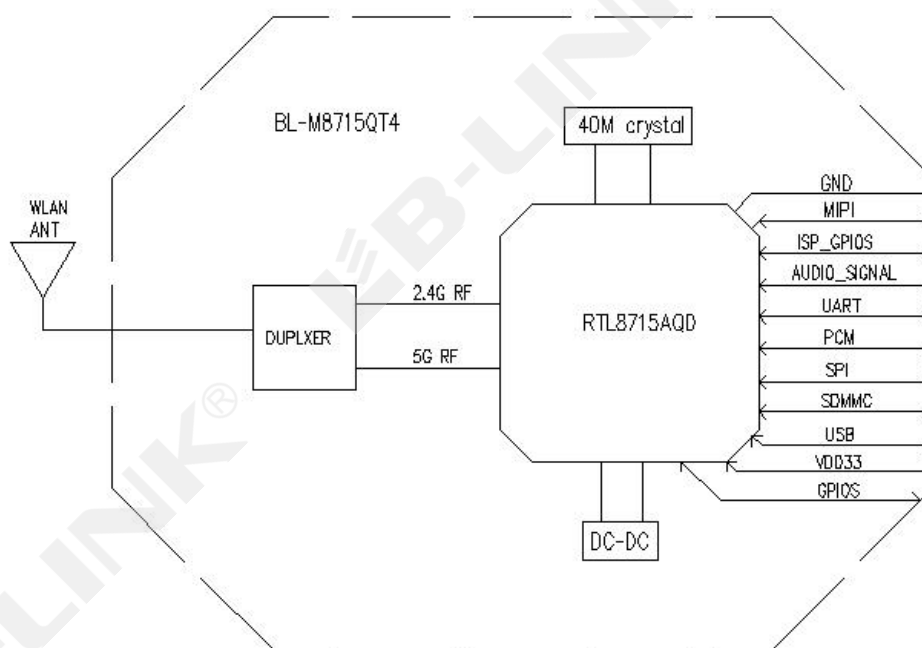
## High speed interface

- USB 2.0 host HS/FS or USB 2.0 device HS/FS selectable
- SDMMC 3.0 with DDR-50/SDR-50 mode or SDIO device 2.0 with SDR25 supported
- IEEE 802.3/u compliant RMII interface can support both PHY/MAC mode

## Peripheral interfaces

- Support 5 UART with multiple selectable interfaces, max baud rate 4MHz
- Support I2S and PCM with multiple selectable interfaces
- MAX 4 I2C with 3-speeds, either master or slave mode supported
- MAX 2 SPI interfaces with master or slave mode supported
- MAX 3 ADC with 10-bit mode and 32KHz sample rate

## 1.3 Block Diagram

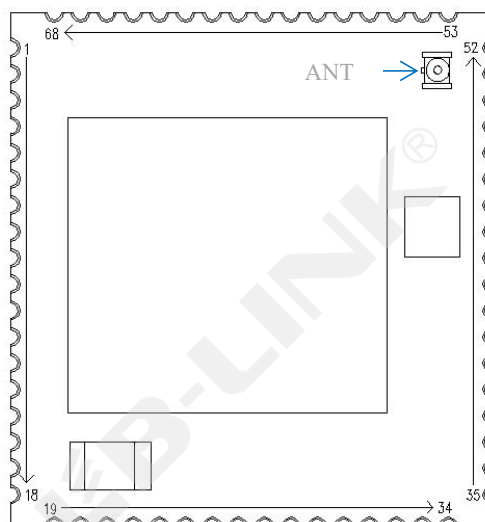


## 1.4 General Specifications

|                |                                        |
|----------------|----------------------------------------|
| Module Name    | BL-M8715QT4 Camera Module              |
| Chipset        | RTL8715AQD-VR3-CG                      |
| WLAN Standards | IEEE802.11b/g/n/ac, 1T1R 150Mbps (Max) |

|                       |                                                                 |
|-----------------------|-----------------------------------------------------------------|
| Bus Protocol          | NOR Flash/SPI/USB2.0 /Audio/UART/MIPI/ISP/I2C/I2S/SDMMC/MII/PCM |
| Antenna               | Connect to external antenna through IPEX-4 connector            |
| Dimension             | SMD 68Pins, 17.6*16.5*1.8mm (L*W*H) ±0.15mm                     |
| Power Supply          | DC 3.3V±0.2V @ 500 mA (Max)                                     |
| Operation Temperature | -20°C to +85°C                                                  |
| Operation Humidity    | 10% to 95% RH (Non-Condensing)                                  |

## 2. Pin Assignments



(Top View)

### 2.1 Pin Definition

| No | Pin Name | Type | Description                                                                                                                                                                                                                                                                                                                                                 | I/O Level |
|----|----------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
|    | ANT      | RF   | 2.4&5G RF port (connect to ant by IPEX-4 connector)                                                                                                                                                                                                                                                                                                         |           |
| 1  | GPIOG_3  | I/O  | GPIOG_3 pin. The MUX function shows below:<br>1. SPI: MISO1_1, SPI Master Input Slave Output signal<br>2. HS-UART: CTS1_1, High-Speed domains UART Clear To Send input signal<br>3. HS-PWM: PWM1_1, High-Speed domains Pulse Width Modulation output signal<br>4. I2S: MCKO_1, I2S Main Clock output(master) signal<br>5. PCM: INO_1, PCM Input data signal | 3.3V      |

|    |           |     |                                                                                                                                                                                                                                                                                                                                                                                   |      |
|----|-----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| 2  | GPIOG_2   | I/O | <p>GPIOG_2 pin. The MUX function shows below:</p> <ol style="list-style-type: none"> <li>1. SPI: MOSI1_1, SPI Master Output Slave Input signal</li> <li>2. HS-UART: RTS1_1, HS-UART Request To Send output signal</li> <li>3. HS-PWM: PWM0_1, HS-PWM output signal</li> <li>4. I2S: TX00_1, I2S TX Data0 output signal</li> <li>5. PCM: OUT0_1, PCM Output Data signal</li> </ol> | 3.3V |
| 3  | GPIOG_1   | I/O | <p>GPIOG_1 pin. The MUX function shows below:</p> <ol style="list-style-type: none"> <li>1. SDMMC: WP0_2, SD Card Write Protection input signal</li> <li>2. SPI: SCL1_1, SPI Serial Clock output(master) signal</li> <li>3. I2S: CLK0_1, I2S Clock output(master) signal</li> <li>4. PCM: CLK0_1, PCM Clock output(master) signal</li> </ol>                                      | 3.3V |
| 4  | GPIOG_0   | I/O | <p>GPIOG_0 pin. The MUX function shows below:</p> <ol style="list-style-type: none"> <li>1. SDMMC: CD0_2, SD Card Detect input signal</li> <li>2. SPI: CS1_1, SPI Chip Select output(master) signal</li> <li>3. I2S: WSO_1, I2S Word Select output(master) signal</li> <li>4. PCM: SYNC0_1, PCM Synchronization output(master) signal</li> </ol>                                  | 3.3V |
| 5  | FLASH_D2  | I/O | <p>GPIOF_10 pin. The MUX function shows below:</p> <ol style="list-style-type: none"> <li>1. FLASH: DATA2, QPI/SPI NOR Flash Data2 I/O signal / Write Protection active low output signal</li> <li>2. SDMMC: CD0_1, SD Card Detect input signal</li> <li>3. HS-I2C: SDA3_2, I2C Serial Data I/O signal</li> </ol>                                                                 | 1.8V |
| 6  | FLASH_D1  | I/O | <p>GPIOF_9 pin. The MUX function shows below:</p> <ol style="list-style-type: none"> <li>1. FLASH: DATA1, QPI/SPI NOR Flash Data1 I/O signal / MISO input signal</li> </ol>                                                                                                                                                                                                       | 1.8V |
| 7  | FLASH_CS  | I/O | <p>GPIOF_7 pin. The MUX function shows below:</p> <ol style="list-style-type: none"> <li>1. FLASH: CS, QPI/SPI NOR Flash Chip Select active low output signal</li> </ol>                                                                                                                                                                                                          | 1.8V |
| 8  | FLASH_D3  | I/O | <p>GPIOF_4 pin. The MUX function shows below:</p> <ol style="list-style-type: none"> <li>1. FLASH: DATA3, QPI/SPI NOR Flash Data3 I/O signal / Hold active low output signal</li> <li>2. SDMMC: WP0_1, SD Card Write Protection input signal</li> <li>3. HS-I2C: SCL3_2, I2C Serial Clock output(master) signal</li> </ol>                                                        | 1.8V |
| 9  | FLASH_CLK | I/O | <p>GPIOF_3 pin. The MUX function shows below:</p> <ol style="list-style-type: none"> <li>1. FLASH: CLK, QPI/SPI NOR Flash Clock output signal</li> </ol>                                                                                                                                                                                                                          | 1.8V |
| 10 | FLASH_D0  | I/O | <p>GPIOF_0 pin. The MUX function shows below:</p> <ol style="list-style-type: none"> <li>1. FLASH: DATA0, QPI/SPI NOR Flash Data0 I/O signal / MOSI output signal</li> </ol>                                                                                                                                                                                                      | 1.8V |

|    |        |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |            |
|----|--------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|
| 11 | VDD18  | P   | 1.8V Power output for external (on customer's mainboard) QPI/SPI NOR Flash only, do not use for other circuits                                                                                                                                                                                                                                                                                                                                                                                                                                            |            |
| 12 | GND    | P   | Ground connections                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |            |
| 13 | SD_CD  | I/O | GPIOB_6 pin. The MUX function shows below:<br>1. SDMMC: CD0_0, SD Card Detect input signal<br>2. SDIO: INT, SDIO Device Interrupt output signal<br>3. HS-PWM: PWM6_3, HS-PWM output signal<br>4. I2S: RX1_0, I2S RX Data input signal                                                                                                                                                                                                                                                                                                                     | 3.3V/1.8V* |
| 14 | SD_D1  | I/O | GPIOB_5 pin. The MUX function shows below:<br>1. SDMMC: D1, SD Card Data1 I/O signal<br>2. SDIO: D1, SDIO Device Data1 I/O signal<br>3. HS-I2C: SCL3_0, I2C Serial Clock output(master) signal<br>4. HS-SGPIO: RX0_0, HS-SGPIO RX input signal<br>5. HS-PWM: PWM5_3, HS-PWM output signal<br>6. I2S: TX21_0, I2S TX Data2 output signal<br>7. RMII: TXEN_0, RMII TX Enable output signal                                                                                                                                                                  | 3.3V/1.8V* |
| 15 | SD_D0  | I/O | GPIOB_4 pin. The MUX function shows below:<br>1. SDMMC: D0, SD Card Data0 I/O signal<br>2. SDIO: D0, SDIO Device Data0 I/O signal<br>3. HS-I2C: SDA3_0, I2C Serial Data I/O signal<br>4. HS-SGPIO: TX0_0, HS-SGPIO TX output signal<br>5. HS-PWM: PWM4_3, HS-PWM output signal<br>6. I2S: TX11_0, I2S TX Data1 output signal                                                                                                                                                                                                                              | 3.3V/1.8V* |
| 16 | SD_CLK | I/O | GPIOB_3 pin. The MUX function shows below:<br>1. SDMMC: CLK, SD Card Clock output signal<br>2. SDIO: CLK, SDIO Device Clock input signal<br>3. SPI: MISO2_0, SPI Master Input Slave Output signal<br>4. HS-I2C: SCL2_0, I2C Serial Clock output(master) signal<br>5. HS-UART: RTS1_0, HS-UART Request To Send output signal<br>6. HS-PWM: PWM3_3, HS-PWM output signal<br>7. I2S: MCK1_0, I2S Main Clock output(master) signal<br>8. PCM: IN1_0, PCM Input Data signal<br>9. RMII: TXCK_0, RMII TX Clock input(MAC mode) signal / output(PHY mode) signal | 3.3V/1.8V* |
| 17 | SD_CMD | I/O | GPIOB_2 pin. The MUX function shows below:<br>1. SDMMC: CMD, SD Card Command I/O signal<br>2. SDIO: CMD, SDIO Device Command I/O signal<br>3. SPI: MOSI2_0, SPI Master Output Slave Input signal<br>4. HS-I2C: SDA2_0, I2C Serial Data I/O signal                                                                                                                                                                                                                                                                                                         | 3.3V/1.8V* |

|    |          |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |
|----|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|
|    |          |     | 5. HS-UART: CTS1_0, HS-UART Clear To Send input signal<br>6. HS-PWM: PWM2_3, HS-PWM output signal<br>7. I2S: TX01_0, I2S TX Data0 output signal<br>8. PCM: OUT1_0, PCM Output Data signal<br>9. RMII: TXD0_0, RMII TX Data0 output signal                                                                                                                                                                                                                                                                      |            |
| 18 | SD_D3    | I/O | GPIOB_1 pin. The MUX function shows below:<br>1. SDMMC: D3, SD Card Data3 I/O signal<br>2. SDIO: D3, SDIO Device Data3 I/O signal<br>3. SPI: SCL2_0, SPI Serial Clock output(master) signal<br>4. HS-I2C: SCL0_0, I2C Serial Clock output(master) signal<br>5. HS-UART: OUT1_0, HS-UART TX Data output signal<br>6. HS-PWM: PWM1_3, HS-PWM output signal<br>7. I2S: CLK1_0, I2S Clock output(master) signal<br>8. PCM: CLK1_0, PCM Clock output(master) signal<br>9. RMII: TXD1_0, RMII TX Data1 output signal | 3.3V/1.8V* |
| 19 | SD_D2    | I/O | GPIOB_0 pin. The MUX function shows below:<br>1. SDMMC: D2, SD Card Data2 I/O signal<br>2. SDIO: D2, SDIO Device Data2 I/O signal<br>3. SPI: CS2_0, SPI Chip Select output(master) signal<br>4. HS-I2C: SDA0_0, I2C Serial Data I/O signal<br>5. HS-UART: IN1_0, HS-UART RX Data input signal<br>6. HS-PWM: PWM0_3, HS-PWM output signal<br>7. I2S: WS1_0, I2S Word Select output(master) signal<br>8. PCM: SYNC1_0, PCM Synchronization output(master) signal                                                 | 3.3V/1.8V* |
| 20 | VDD33    | P   | 3.3V Main power supply                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |            |
| 21 | VDD33    | P   | 3.3V Main power supply                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |            |
| 22 | GND      | P   | Ground connections                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |            |
| 23 | AOUT_P   | AO  | Speaker single-ended output signal                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |            |
| 24 | GND      | P   | Ground connections                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |            |
| 25 | MIC_BIAS | AO  | Microphone bias output                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |            |
| 26 | MIC_P    | AI  | Microphone single-ended input signal                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |            |
| 27 | GND      | P   | Ground connections                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |            |
| 28 | MDN0     | AI  | GPIOB_15 pin. The MUX function shows below:<br>1. MIPI: DATA0_N, MIPI Sensor lane0 differential data negative input signal                                                                                                                                                                                                                                                                                                                                                                                     | 3.3V       |
| 29 | MDP0     | AI  | GPIOB_14 pin. The MUX function shows below:<br>1. MIPI: DATA0_P, MIPI Sensor lane0 differential data positive input signal                                                                                                                                                                                                                                                                                                                                                                                     | 3.3V       |

|    |          |          |                                                                                                                                                                                                                              |      |
|----|----------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| 30 | MCN      | AI       | GPIOD_13 pin. The MUX function shows below:<br>1. MIPI: CLI_N, MIPI Sensor differential clock negative input signal                                                                                                          | 3.3V |
| 31 | MCP      | AI       | GPIOD_12 pin. The MUX function shows below:<br>1. MIPI: CKI_P, MIPI Sensor differential clock positive input signal                                                                                                          | 3.3V |
| 32 | MDN1     | AI       | GPIOD_11 pin. The MUX function shows below:<br>1. MIPI: DATA1_N, MIPI Sensor lane1 differential data negative input signal                                                                                                   | 3.3V |
| 33 | MDP1     | AI       | GPIOD_10 pin. The MUX function shows below:<br>1. MIPI: DATA1_P, MIPI Sensor lane1 differential data positive input signal                                                                                                   | 3.3V |
| 34 | GND      | P        | Ground connections                                                                                                                                                                                                           |      |
| 35 | HSDM     | A<br>I/O | USB2.0 High-Speed differential data negative signal                                                                                                                                                                          |      |
| 36 | HSDP     | A<br>I/O | USB2.0 High-Speed differential data positive signal                                                                                                                                                                          |      |
| 37 | GND      | P        | Ground connections                                                                                                                                                                                                           |      |
| 38 | SEN_SDA  | O        | GPIOD_1 pin. The MUX function shows below:<br>1. ISP-I2C: SDA0_0, I2C Serial Data I/O signal, dedicated for COMS Sensor management                                                                                           | 3.3V |
| 39 | SEN_SCL  | I/O      | GPIOD_0 pin. The MUX function shows below:<br>1. ISP-I2C: SCL0_0, I2C Serial Clock output signal, dedicated for COMS Sensor management                                                                                       | 3.3V |
| 40 | GPIOE_0  | I/O      | GPIOE_0 pin. The MUX function shows below:<br>1. HS-UART: INT2_1, HS-UART RX Data input signal<br>2. HS-PWM: PWM0_0, HS-PWM output signal<br>3. RMII: RXCK_0, RMII RX Clock input(MAC mode) signal / output(PHY mode) signal | 3.3V |
| 41 | GPIOE_2  | I/O      | GPIOE_2 pin. The MUX function shows below:<br>1. HS-PWM: PWM2_0, HS-PWM output signal<br>2. RMII: RXD1_0, RMII RX Data1 input signal                                                                                         | 3.3V |
| 42 | GPIOE_1  | I/O      | GPIOE_1 pin. The MUX function shows below:<br>1. HS-UART: OUT2_1, HS-UART TX Data output signal<br>2. HS-PWM: PWM1_0, HS-PWM output signal<br>3. RMII: RXD0_0, RMII RX Data0 input signal                                    | 3.3V |
| 43 | GPIOE_14 | I/O      | GPIOE_14 pin. The MUX function shows below:<br>1. HS-I2C: SDA2_2, I2C Serial Data I/O signal<br>2. HS-SGPIO: TX2_2, HS-SGPIO TX output signal                                                                                | 3.3V |
| 44 | GPIOE_15 | I/O      | GPIOE_15 pin. The MUX function shows below:<br>1. HS-I2C: SCL2_2, I2C Serial Clock output(master)                                                                                                                            | 3.3V |

|    |            |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |      |
|----|------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
|    |            |     | signal<br>2. HS-SGPIO: RX2_2, HS-SGPIO RX input signal                                                                                                                                                                                                                                                                                                                                                                                                                                                |      |
| 45 | SEN_SYSCLK | I/O | GPIOE_13 pin. The MUX function shows below:<br>1. ISP Control: SSOR_SYSCLK0_1, Sys_Clock output signal for Sensor                                                                                                                                                                                                                                                                                                                                                                                     | 3.3V |
| 46 | GPIOA_0    | I/O | Low Power Domain GPIOA_0 pin. The MUX function shows below:<br>1. LP-ADC: ADC0_0, AD converter input channel 0<br>2. LP-UART: IN1_0, LP-UART RX Data input signal<br>3. LP-PWM: PWM0_0, LP-PWM output signal<br>4. LP-QDEC: PHA0_0                                                                                                                                                                                                                                                                    | 3.3V |
| 47 | GPIOA_1    | I/O | Low Power Domain GPIOA_1 pin. The MUX function shows below:<br>1. LP-ADC: ADC1_0, AD converter input channel 1<br>2. LP-UART: OUT1_0, LP-UART TX Data output signal<br>3. LP-PWM: PWM1_0, LP-PWM output signal<br>4. LP-QDEC: PHB0_0                                                                                                                                                                                                                                                                  | 3.3V |
| 48 | GPIOA_2    | I/O | Function_A. "UART_IMAGE_DLOAD" Boot strap :<br>0 : RTK reserved<br>1: Download image from UART(Internal pulled high by 10K).<br>Note: Only valid when "NORMAL_MODE_SEL"=1, and do not care when "NORMAL_MODE_SEL"=0.<br>Function_B. Low Power Domain GPIOA_2 pin. The MUX function shows below:<br>1. LP-ADC: ADC2_0, AD converter input channel 2<br>2. LP-UART: CTS1_0, LP-UART Clear To Send input signal<br>3. LP-PWM: PWM2_0, LP-PWM output signal<br>4. LP-QDEC: IDX0_0                         | 3.3V |
| 49 | GPIOA_8    | I/O | Function_A. "EEPROM_SEL" Boot strap :<br>0: Internal NV memory select (Internal pulled low by 10K)<br>1: Reserved for internal testing use<br>Function_B. Low Power Domain GPIOA_8 pin. The MUX function shows below:<br>1. LP-SWD: SDIO, SWD data signal<br>2. LP-UART: OUT0_0, LP-UART TX Data output signal<br>3. LP-I2C: SDA0_2, I2C Serial Data I/O signal<br>4. LP-SGPIO: TX0_1, LP-SGPIO TX output signal<br>5. LP-PWM: PWM1_1, LP-PWM output signal<br>6. LP-QDEC: IDX0_1<br>7. LP-CIR: TX0_0 | 3.3V |

|    |               |     |                                                                                                                                                                                                                                                                                                                                                      |      |
|----|---------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| 50 | GPIOA_7       | I/O | Low Power Domain GPIOA_7 pin. The MUX function shows below:<br>1. LP-SWD: SCK, SWD clock signal<br>2. LP-UART: IN0_0, LP-UART RX Data input signal<br>3. LP-I2C: SCL0_2, I2C Serial Clock output(master) signal<br>4. LP-SGPIO: RX0_1, HS-SGPIO RX input signal<br>5. LP-PWM: PWM0_1, LP-PWM output signal<br>6. LP-QDEC: PHB0_1<br>7. LP-CIR: RX0_0 | 3.3V |
| 51 | GPIOA_13      | I/O | Low Power Domain GPIOA_13 pin. The MUX function shows below:<br>1. LP-PWM: PWM7_0, LP-PWM output signal<br>2. LP-QDEC: PHA0_1<br>3. DSLP_WAKE: DSLP_Wake                                                                                                                                                                                             | 3.3V |
| 52 | TEST_MD_SEL   | I/O | Function_A. "NORMAL_MODE_SEL" Boot strap :<br>0: Normal operation mode (internal pulled low by 10K )<br>1: Enter into test/debug mode<br>Function_B. Low Power Domain GPIOA_9 pin. The MUX function shows below:<br>1. LP-PWM: PWM2_1, LP-PWM output signal                                                                                          | 3.3V |
| 53 | GND           | P   | Ground connections                                                                                                                                                                                                                                                                                                                                   |      |
| 54 | GND           | P   | Ground connections                                                                                                                                                                                                                                                                                                                                   |      |
| 55 | GND           | P   | Ground connections                                                                                                                                                                                                                                                                                                                                   |      |
| 56 | SENSOR_PDN    | I/O | GPIOC_3 pin. The MUX function shows below:<br>1. ISP control: GPIO1_1, used as Sensor Power Down Enable output signal                                                                                                                                                                                                                                | 3.3V |
| 57 | SENSOR_RSTB   | I/O | GPIOC_2 pin. The MUX function shows below:<br>1. ISP control: GPIO0_1, used as Sensor Reset output signal                                                                                                                                                                                                                                            | 3.3V |
| 58 | GPIOC_10      | I/O | GPIOC_10 pin. The MUX function shows below:<br>1. HS-UART: CTS2_0, HS-UART Clear To Send input signal<br>2. HS-PWM: PWM6_2, HS-PWM output signal<br>3. RMII: MDC_0, SMI Clock output signal<br>4. RF control I/O: RFCTRL2_0, WLAN RF Front-End Control output signal 2                                                                               | 3.3V |
| 59 | SENSOR_PWR_EN | I/O | GPIOC_4 The MUX function shows below:<br>1. HS-PWM: PWM0_2, HS-PWM output signal<br>2. ISP control: GPIO2_1, used as Sensor Power Enable output signal                                                                                                                                                                                               | 3.3V |
| 60 | GPIOC_11      | I/O | GPIOC_11 pin. The MUX function shows below:                                                                                                                                                                                                                                                                                                          | 3.3V |

|    |         |     |                                                                                                                                                                                                                                                                                                                                                                                                           |      |
|----|---------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
|    |         |     | <ol style="list-style-type: none"> <li>1. HS-UART: RTS2_0, HS-UART Request To Send output signal</li> <li>2. HS-PWM: PWM7_2, HS-PWM output signal</li> <li>3. RMI: MDIO_0, SMI Serial Data I/O signal</li> <li>4. RF control I/O: RFCTRL3_0, WLAN RF Front-End Control output signal 3</li> </ol>                                                                                                         |      |
| 61 | GPIOC_9 | I/O | <p>GPIOC_9 pin. The MUX function shows below:</p> <ol style="list-style-type: none"> <li>1. HS-UART: OUT2_0, HS-UART TX Data output signal</li> <li>2. HS-SGPIO: RX1_0, HS-SGPIO RX input signal</li> <li>3. HS-PWM: PWM5_2, HS-PWM output signal</li> <li>4. RF control I/O: RFCTRL1_0, WLAN RF Front-End Control output signal 1</li> <li>5. LED: LED0_3, Status indicator LED output signal</li> </ol> | 3.3V |
| 62 | GPIOC_8 | I/O | <p>GPIOC_8 pin. The MUX function shows below:</p> <ol style="list-style-type: none"> <li>1. HS-UART: IN2_0, HS-UART RX Data input signal</li> <li>2. HS-SGPIO: TX1_0, HS-SGPIO TX output signal</li> <li>3. HS-PWM: PWM4_2, HS-PWM output signal</li> <li>4. RF control I/O: RFCTRL0_0, WLAN RF Front-End Control output signal 0</li> <li>5. LED: LED0_2, Status indicator LED output signal</li> </ol>  | 3.3V |
| 63 | GPIOG_9 | I/O | <p>GPIOG_9 pin. The MUX function shows below:</p> <ol style="list-style-type: none"> <li>1. HS-PWM: PWM7_1, HS-PWM output signal</li> </ol>                                                                                                                                                                                                                                                               | 3.3V |
| 64 | GPIOG_8 | I/O | <p>GPIOG_8 pin. The MUX function shows below:</p> <ol style="list-style-type: none"> <li>1. HS-PWM: PWM6_1, HS-PWM output signal</li> </ol>                                                                                                                                                                                                                                                               | 3.3V |
| 65 | LOG_IN  | I/O | <p>GPIOG_6 pin. The MUX function shows below:</p> <ol style="list-style-type: none"> <li>1. HS-I2C: SDA2_1, I2C Serial Data I/O signal</li> <li>2. HS-UART: IN0_1, HS-UART RX Data input signal used for software Log and debug</li> <li>3. HS-PWM: PWM4_1, HS-PWM output signal</li> <li>4. I2S: RX0_1, I2S RX Data input signal</li> </ol>                                                              | 3.3V |
| 66 | LOG_OUT | I/O | <p>GPIOG_7 pin. The MUX function shows below:</p> <ol style="list-style-type: none"> <li>1. HS-I2C: SCL2_1, I2C Serial Clock output(master) signal</li> <li>2. HS-UART: OUT0_1, HS-UART TX Data output signal used for software Log and debug</li> <li>3. HS-PWM: PWM5_1, HS-PWM output signal</li> </ol>                                                                                                 | 3.3V |
| 67 | GPIOG_5 | I/O | <p>GPIOG_5 pin. The MUX function shows below:</p> <ol style="list-style-type: none"> <li>1. HS-I2C: SCL0_1, I2C Serial Clock output(master) signal</li> <li>2. HS-UART: IN1_1, HS-UART RX Data input signal</li> <li>3. HS-PWM: PWM3_1, HS-PWM output signal</li> <li>4. I2S: TX20_1, I2S TX Data2 output signal</li> </ol>                                                                               | 3.3V |

|    |         |     |                                                                                                                                                                                                                                           |      |
|----|---------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| 68 | GPIOG_4 | I/O | GPIOG_4 pin. The MUX function shows below:<br>1. HS-I2C: SDA0_1, I2C Serial Data I/O signal<br>2. HS-UART: OUT1_1, HS-UART TX Data output signal<br>3. HS-PWM: PWM2_1, HS-PWM output signal<br>4. I2S: TX10_1, I2S TX Data1 output signal | 3.3V |
|----|---------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|

P: Power or Ground; I/O: In/Output; I: Input; O: Output; O/D: Open Drain Output; A I/O: Analog In/Output; AI: Analog Input; AO: Analog Output; RF: Analog RF Port or RF Ground;

Note: The unused GPIO pins are suggested to keep floating.

Every GPIO pin can be selected as interrupt source and can enable Schmitt trigger if needing.

Default states of all GPIO pins are High-impedance and can be configured Pull-High and Pull-Low in Sleep mode.

3.3V/1.8V\*: Depends on the working mode and voltage negotiated between SD/SDIO Host and Device

## 2.2 Function Group Summary

| Function | Group                  | Description                             | Specifications                                                                                                                                                     | Usage |
|----------|------------------------|-----------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| SWD      | SWD                    | SWD interface                           | Low-power domains Serial Wire Debug interface                                                                                                                      |       |
| ADC      | ADC0~3                 | Low power ADC                           | 10-bit resolution, 32KHz bandwidth                                                                                                                                 |       |
|          | ADBAT                  | Dedicated ADC pin                       | Dedicated ADC pin for USB_5V or Vbat                                                                                                                               |       |
| UART     | LP-UART0_0, LP-UART1_0 | LP-UART0_0(2-wire) & LP-UART1_0(4-wire) | Two independent low-power domains UART: 4-wire UART interface with RX, TX, CTS and RTS. 2-wire UART interface with RX and TX. The default baud rate is 115.2k baud |       |
|          | HS-UART0_1             | HS-UART0_1(2-wire)                      | Independent high-speed domains UART, max baud rate 4MHz and DMA mode, used for software Log and debug                                                              |       |
|          | HS-UART1_0/HS-UART1_1  | HS-UART1_0(4-wire) / HS-UART1_1(4-wire) | Independent high-speed domains UART with two selectable 4-wire interfaces, max baud rate 4MHz and DMA mode                                                         |       |
|          | HS-UART2_0/HS-UART2_1  | HS-UART2_0(4-wire) / HS-UART2_1(2-wire) | Independent high-speed domains UART with a 4-wire and a 2-wire selectable interfaces, max baud rate 4MHz and DMA mode                                              |       |
| I2C      | LP-I2C0_2              | Either I2C master or slave              | Independent low-power domains I2C, support 3-speeds: Standard mode (0~100kb/s), Fast mode (<400kb/s),                                                              |       |

|             |                                       |                                            |                                                                                                                                                          |  |
|-------------|---------------------------------------|--------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------|--|
|             |                                       |                                            | High-speed mode (<3.4Mb/s with appropriate bus loading), support 7/10bit addressing                                                                      |  |
|             | HS-I2C0_0/<br>HS-I2C0_1               | Either I2C master or slave                 | Independent high-speed domains I2C with multiple selectable interfaces, support 3-speeds and 7/10bit addressing                                          |  |
|             | HS-I2C2_0/<br>HS-I2C2_1/<br>HS-I2C2_2 | Either I2C master or slave                 |                                                                                                                                                          |  |
|             | HS-I2C3_0/<br>HS-I2C3_2               | Either I2C master or slave                 |                                                                                                                                                          |  |
| SGPIO       | LP-SGPIO0_1                           | Low-power domain SGPIO                     | multiple selectable interfaces and support multiple working modes                                                                                        |  |
|             | HS-SGPIO0_0                           | high-speed domain SGPIO                    |                                                                                                                                                          |  |
|             | HS-SGPIO1_0                           |                                            |                                                                                                                                                          |  |
|             | HS-SGPIO2_2                           |                                            |                                                                                                                                                          |  |
| PWM         | LP-PWM0_0/0_1<br>/1_0/1_1/2_0/2_1/7_0 | Low-power domains PWM                      | Support Max 8-PWM functions at LP/HS domain with multiple selectable pins. 0~100% duty can be configurable, selected Gtimer interrupt as counter source. |  |
|             | HS-PWM0_0/0_2/1_0/2_0/4~7_2/0~6_3     | High-speed domains PWM                     |                                                                                                                                                          |  |
| USB         | HSDM、HSDP                             | USB Device interface                       | Support HS/FS/LS modes, up to 480Mbps, up to 4-Endpoints in addition to Endpoint0                                                                        |  |
|             |                                       | USB Host interface                         | Support HS/FS/LS modes, up to 480Mbps ,support up to 8 host channels                                                                                     |  |
| QDEC        | LP-QDEC                               | Quadrature decoder interface               | Low-power domains quadrature decoder interface. Support 16-bits position counter, velocity counter and 12-bits rotation counter                          |  |
| CIR         | LP-CIR                                | Infrared Radiation communication interface | Support IR diode/module input and output. Make de-modulation and encode symbols for RX, make decode symbols and modulation for TX                        |  |
| DSL_P_WAK E | DSL_P_WAKE                            | DSL_P_WAKE input pin                       | This DSL_P_WAKE external input signal can wake the module entering deep sleep mode                                                                       |  |
| SDIO        | SDIO                                  | SDIO device mode only                      | Support SDIO 2.0 SDR25                                                                                                                                   |  |
| SD CARD     | SDMMC                                 | SDMMC interface                            | Support SDMMC 3.0 with up to DDR-50/SDR-50 mode                                                                                                          |  |

|             |                               |                                                   |                                                                                                                                                               |                                                                                                                                                                           |
|-------------|-------------------------------|---------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| FLASH       | SPI NOR FLASH                 | SPI NOR FLASH Controller                          | Targeted SPI Nor Flash frequency up to 75MHz (Quad IO QPI Nor Flash with SDR 75MHz and DTR 50MHz)                                                             | Supported 32Mbit 1.8V Quad I/O SPI Nor Flash: W25Q32JW                                                                                                                    |
| SPI         | SPI1_1                        | Either SPI master or slave                        | Support Moto SPI, TI SSP and NS Microwire protocol, Master clock up to 75MHz, Slave RX only with 18.75MHz and TX/RX with 9.375MHz                             |                                                                                                                                                                           |
|             | SPI2_0                        | SPI master only                                   | Support Moto SPI protocol only, Master clock up to 37.5MHz                                                                                                    |                                                                                                                                                                           |
| I2S         | I2S0_1                        | Support the master/slave mode                     | Two Selectable interface, support multiple sample rate and bits data length, support 5.1 TX mode (I2S0_1 only)                                                |                                                                                                                                                                           |
|             | I2S1_0                        |                                                   |                                                                                                                                                               |                                                                                                                                                                           |
| PCM         | PCM0_1                        | Independently operate in the master or slave mode | Two Selectable interface, the sample rate is 8KHz, support the 8-bit companding mode and 16-bit liner mode, support 16 independent channels and 32 time slots |                                                                                                                                                                           |
|             | PCM1_0                        |                                                   |                                                                                                                                                               |                                                                                                                                                                           |
| ISP CONTROL | ISP-I2C0_0                    | I2C for ISP control                               | Dedicated I2C for COMS sensor                                                                                                                                 |                                                                                                                                                                           |
|             | ISP-GPIO0_1/1_1/2_1           | I/O for ISP control                               | GPIO used as COMS sensor Reset, power enable, power down control signal                                                                                       |                                                                                                                                                                           |
|             | SSOR_SYCLK0_1                 | I/O for ISP control                               | Used as clock output signal for COMS sensor                                                                                                                   |                                                                                                                                                                           |
|             | MIPI-DATA0_1, CLK_P/N         | MIPI CSI-2 two data lane interface                | Two differential data lane and one differential clock lane interface, from the COMS sensor                                                                    |                                                                                                                                                                           |
| RMII        | MDC/MDIO_0                    | SMI master interface                              | SMI interface can be used for external Ethernet PHY management                                                                                                | The RXDV signal is pulled high by 10K resistance inside the module and it is not led out for customer. Therefore, the TXEN output signal of RMII device on the customer's |
|             | TXD0~1\TXCK\TXEN, RXD0~1\RXCK | RMII interface support both PHY/MAC mode          | IEEE802.3/802.3u compliant, support 10/100Mbps half/full duplex Auto negotiation                                                                              |                                                                                                                                                                           |

|            |               |                                    |                                      |                                                          |
|------------|---------------|------------------------------------|--------------------------------------|----------------------------------------------------------|
|            |               |                                    |                                      | motherboard cannot be connected to it , will be floating |
| RF CONTROL | RFCTRL0~3_0   | I/O for WLAN RF Front-End control  | 4-I/Os for WLAN RF Front-End control |                                                          |
| LED        | LED0_2/LED0_3 | Status indicator LED output signal | 2 status indicator LED output signal |                                                          |

## 3. Electrical and Thermal Specifications

### 3.1 Recommended Operating Conditions

| Parameters                              |                                    | Min  | Typ | Max  | Units |
|-----------------------------------------|------------------------------------|------|-----|------|-------|
| Ambient Operating Temperature           |                                    | -20  | 25  | 85   | °C    |
| * limited Ambient Operating temperature |                                    | -40  | 25  | 85   | °C    |
| Storage temperature                     |                                    | -40  | 25  | 85   | °C    |
| External Antenna VSWR                   |                                    | --   | 1.7 | 2    | /     |
| Supply Voltage                          | VDD33                              | 3.1  | 3.3 | 3.5  | V     |
|                                         | VDD18 (Output for external Flash ) | 1.75 | 1.8 | 1.95 | V     |

Note: \* The module has passed the minimum system operation test and WLAN communication test under this temperature range, but it cannot completely guarantee that the overall function composed of external circuits can also pass the test.

### 3.2 Digital I/O DC Specifications

| Symbol          | Parameter           | Min | Typ | Max | Units |
|-----------------|---------------------|-----|-----|-----|-------|
| <b>3.3V I/O</b> |                     |     |     |     |       |
| VIH             | Input High Voltage  | 2   | --  | --  | V     |
| VIL             | Input Low Voltage   | --  | --  | 0.8 | V     |
| VOH             | Output High Voltage | 2.4 | --  | --  | V     |

|                 |                     |      |    |      |   |
|-----------------|---------------------|------|----|------|---|
| VOL             | Output Low Voltage  | --   | -- | 0.4  | V |
| <b>1.8V I/O</b> |                     |      |    |      |   |
| VIH             | Input High Voltage  | 1.3  | -- | --   | V |
| VIL             | Input Low Voltage   | --   | -- | 0.3  | V |
| VOH             | Output High Voltage | 1.62 | -- | --   | V |
| VOL             | Output Low Voltage  | --   | -- | 0.18 | V |

### 3.3 Current Consumption

| Conditions : VDD33=3.3V ; Ta:25°C ;          |                         |     |       |
|----------------------------------------------|-------------------------|-----|-------|
| Use Case : Minimum System under WLAN RF Test | VDD33 Current (average) |     |       |
|                                              | Typ                     | Max | Units |
| 2.4G 1Mbps TX@17dBm(RF-Test)                 | 290                     | 315 | mA    |
| 2.4G 1Mbps RX(RF-Test)                       | 104                     | 114 | mA    |
| 2.4G 11Mbps TX@17dBm(RF-Test)                | 276                     | 308 | mA    |
| 2.4G 11Mbps RX(RF-Test)                      | 106                     | 116 | mA    |
| 2.4G 6Mbps TX@17dBm(RF-Test)                 | 293                     | 325 | mA    |
| 2.4G 6Mbps RX(RF-Test)                       | 112                     | 122 | mA    |
| 2.4G 54Mbps TX@15dBm(RF-Test)                | 234                     | 266 | mA    |
| 2.4G 54Mbps RX(RF-Test)                      | 110                     | 120 | mA    |
| 2.4G MCS0(HT20) TX@16dBm(RF-Test)            | 302                     | 335 | mA    |
| 2.4G MCS0(HT20) RX(RF-Test)                  | 113                     | 123 | mA    |
| 2.4G MCS7(HT20) TX@14dBm(RF-Test)            | 220                     | 250 | mA    |
| 2.4G MCS7(HT20) RX(RF-Test)                  | 114                     | 124 | mA    |
| 2.4G MCS0(HT40) TX@16dBm(RF-Test)            | 275                     | 310 | mA    |
| 2.4G MCS0(HT40) RX(RF-Test)                  | 117                     | 127 | mA    |
| 2.4G MCS7(HT40) TX@14dBm(RF-Test)            | 203                     | 235 | mA    |

|                                  |     |     |    |
|----------------------------------|-----|-----|----|
| 2.4G MCS7(HT40) RX(RF-Test)      | 117 | 127 | mA |
| 5G 6Mbps TX@16dBm(RF-Test)       | 390 | 420 | mA |
| 5G 6Mbps RX(RF-Test)             | 130 | 140 | mA |
| 5G 54Mbps TX@13dBm(RF-Test)      | 303 | 335 | mA |
| 5G 54Mbps RX(RF-Test)            | 128 | 138 | mA |
| 5G MCS7(HT20) TX@13dBm(RF-Test)  | 300 | 330 | mA |
| 5G MCS7(HT20) RX(RF-Test)        | 130 | 140 | mA |
| 5G MCS0(HT40) TX@16dBm(RF-Test)  | 380 | 410 | mA |
| 5G MCS0(HT40) RX(RF-Test)        | 135 | 144 | mA |
| 5G MCS7(HT40) TX@13dBm(RF-Test)  | 270 | 300 | mA |
| 5G MCS7(HT40) RX(RF-Test)        | 133 | 143 | mA |
| 5G MCS8(VHT20) TX@13dBm(RF-Test) | 256 | 298 | mA |
| 5G MCS8(VHT20) RX(RF-Test)       | 130 | 145 | mA |

## 4. WLAN RF Specification

### 4.1 2.4G WLAN RF Specifications

| Conditions : VDD33=3.3V ; Ta:25°C |                                                                                                                                                                                       |
|-----------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Features                          | Description                                                                                                                                                                           |
| WLAN Standard                     | IEEE 802.11b/g/n                                                                                                                                                                      |
| Frequency Range                   | 2.4~2.4835GHz (2.4GHz ISM Band)                                                                                                                                                       |
| Channels                          | Ch1~Ch13 (For 20MHz Channels)                                                                                                                                                         |
| Modulation                        | 802.11b (DSSS): DBPSK, DQPSK, CCK;<br>802.11g (OFDM): BPSK, QPSK, QAM16, QAM64;<br>802.11n (OFDM): BPSK, QPSK, QAM16, QAM64;                                                          |
| Date Rate                         | 802.11b: 1, 2, 5.5, 11Mbps;<br>802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps;<br>802.11n (HT20): MCS0~MCS7(1T1R_SISO) 6.5~72.2Mbps;<br>802.11n (HT40): MCS0~MCS7(1T1R_SISO) 13.5~150Mbps; |
| Frequency Tolerance               | ≤ ±20ppm                                                                                                                                                                              |

| 2.4G Transmitter Specifications |                                    |                      |        |
|---------------------------------|------------------------------------|----------------------|--------|
| TX Rate                         | TX Power                           | TX Power Tolerance   | EVM    |
| 802.11b@1Mbps                   | Recommended Target TX Power =17dBm | ±2dBm                | ≤-10dB |
| 802.11b@11Mbps                  | Calibrated TX Power =17dBm         | ±2dBm                | ≤-10dB |
| 802.11g@6Mbps                   | Recommended Target TX Power ≤17dBm | ±2dBm                | ≤-10dB |
| 802.11g@54Mbps                  | Calibrated TX Power =15dBm         | ±2dBm                | ≤-25dB |
| 802.11n@HT20_MCS0               | Recommended Target TX Power ≤16dBm | ±2dBm                | ≤-10dB |
| 802.11n@HT20_MCS7               | Calibrated TX Power =14dBm         | ±2dBm                | ≤-28dB |
| 802.11n@HT40_MCS0               | Recommended Target TX Power ≤16dBm | ±2dBm                | ≤-10dB |
| 802.11n@HT40_MCS7               | Calibrated TX Power =14dBm         | ±2dBm                | ≤-28dB |
| 2.4G Receiver Specifications    |                                    |                      |        |
| RX Rate                         | Min Input Level(Typ)               | Max Input Level(Typ) | PER    |
| 802.11b@1Mbps                   | -94dBm                             | -10dBm               | < 8%   |
| 802.11b@11Mbps                  | -86dBm                             | -10dBm               | < 8%   |
| 802.11g@6Mbps                   | -90dBm                             | -20dBm               | < 10%  |
| 802.11g@54Mbps                  | -73dBm                             | -20dBm               | < 10%  |
| 802.11n@HT20_MCS0               | -88dBm                             | -20dBm               | < 10%  |
| 802.11n@HT20_MCS7               | -70dBm                             | -20dBm               | < 10%  |
| 802.11n@HT40_MCS0               | -87dBm                             | -20dBm               | < 10%  |
| 802.11n@HT40_MCS7               | -68dBm                             | -20dBm               | < 10%  |

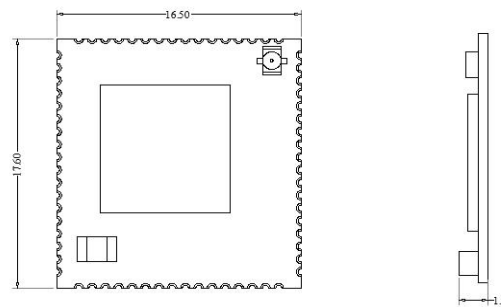
## 4.2 5G WLAN RF Specification

| Conditions : VDD33=3.3V ; Ta:25°C |                                                                                        |
|-----------------------------------|----------------------------------------------------------------------------------------|
| Features                          | Description                                                                            |
| WLAN Standard                     | IEEE 802.11a/n/ac                                                                      |
| Frequency Range                   | 5.15~5.25GHz; 5.25~5.35GHz; 5.47~5.73GHz;<br>5.735~5.835GHz (5GHz ISM Band)            |
| Channels                          | Ch36 , Ch40 , Ch44 , Ch48 ; Ch52~Ch64 ; Ch100~Ch140 ; Ch149~Ch165 (For 20MHz Channels) |

|                               |                                                                                                                                                                                                                              |                      |        |
|-------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|--------|
| Modulation                    | 802.11a (OFDM) : BPSK , QPSK , QAM16 , QAM64 ;<br>802.11n (OFDM) : BPSK , QPSK , QAM16 , QAM64 ;<br>802.11ac (OFDM) : BPSK , QPSK , QAM16 , QAM64 ;                                                                          |                      |        |
| Date Rate                     | 802.11a: 6 , 9 , 12 , 18 , 24 , 36 , 48 , 54Mbps ;<br>802.11n (HT20) : MCS0~MCS7(1T1R_SISO) 6.5~72.2Mbps ;<br>802.11n (HT40) : MCS0~MCS7(1T1R_SISO) 13.5~150Mbps ;<br>802.11ac (VHT20) : MCS0~MCS8(1T1R_SISO) 6.5~86.7Mbps ; |                      |        |
| Frequency Tolerance           | ≤ ±20ppm                                                                                                                                                                                                                     |                      |        |
| 5G Transmitter Specifications |                                                                                                                                                                                                                              |                      |        |
| TX Rate                       | TX Power                                                                                                                                                                                                                     | TX Power Tolerance   | EVM    |
| 802.11a@6Mbps                 | Recommended Target TX Power ≤ 16dBm                                                                                                                                                                                          | ±2dBm                | ≤-10dB |
| 802.11a@54Mbps                | Calibrated TX Power =14dBm                                                                                                                                                                                                   | ±2dBm                | ≤-25dB |
| 802.11n@HT20_MCS0             | Recommended Target TX Power ≤ 16dBm                                                                                                                                                                                          | ±2dBm                | ≤-10dB |
| 802.11n@HT20_MCS7             | Calibrated TX Power =13dBm                                                                                                                                                                                                   | ±2dBm                | ≤-28dB |
| 802.11n@HT40_MCS0             | Recommended Target TX Power ≤ 16dBm                                                                                                                                                                                          | ±2dBm                | ≤-10dB |
| 802.11n@HT40_MCS7             | Calibrated TX Power =13dBm                                                                                                                                                                                                   | ±2dBm                | ≤-28dB |
| 802.11ac@VHT20_MCS8           | Calibrated TX Power =13dBm                                                                                                                                                                                                   | ±2dBm                | ≤-30dB |
| 5G Receiver Specifications    |                                                                                                                                                                                                                              |                      |        |
| RX Rate                       | Min Input Level(Typ)                                                                                                                                                                                                         | Max Input Level(Typ) | PER    |
| 802.11a@6Mbps                 | -88dBm                                                                                                                                                                                                                       | -25dBm               | < 10%  |
| 802.11a@54Mbps                | -69dBm                                                                                                                                                                                                                       | -25dBm               | < 10%  |
| 802.11n@HT20_MCS0             | -86dBm                                                                                                                                                                                                                       | -25dBm               | < 10%  |
| 802.11n@HT20_MCS7             | -66dBm                                                                                                                                                                                                                       | -25dBm               | < 10%  |
| 802.11n@HT40_MCS0             | -84dBm                                                                                                                                                                                                                       | -25dBm               | < 10%  |
| 802.11n@HT40_MCS7             | -65dBm                                                                                                                                                                                                                       | -25dBm               | < 10%  |
| 802.11ac@VHT20_MCS8           | -57dBm                                                                                                                                                                                                                       | -25dBm               | < 10%  |

## 5. Mechanical Specifications

### 5.1 Module Outline Drawing

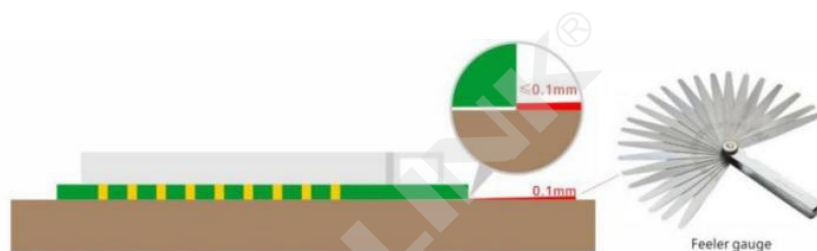


(Top View)

(Side View)

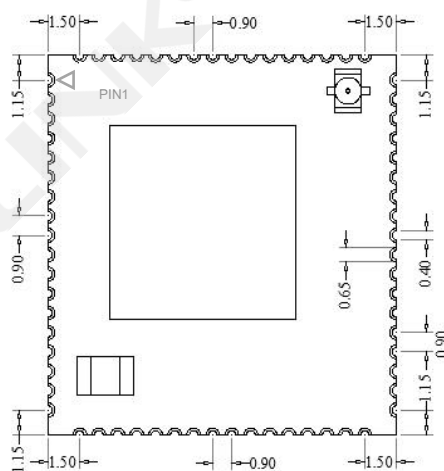
Module dimension: 17.6\*16.5\*1.8mm (L\*W\*H; Tolerance:  $\pm 0.15\text{mm}$ )

IPEX / MHF-4 connector dimension: 2.0\*2.0\*0.6mm (L\*W\*H,  $\varnothing 1.5\text{mm}$ )

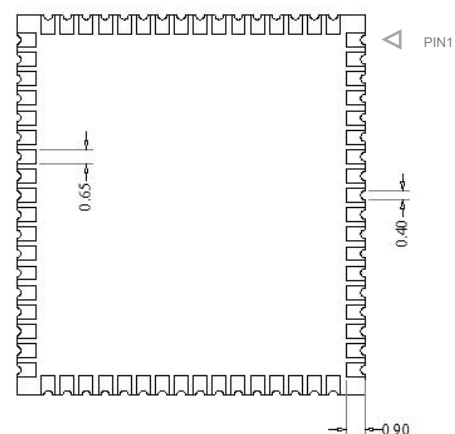


Module Bow and Twist:  $\leq 0.1\text{mm}$

### 5.2 Mechanical Dimensions



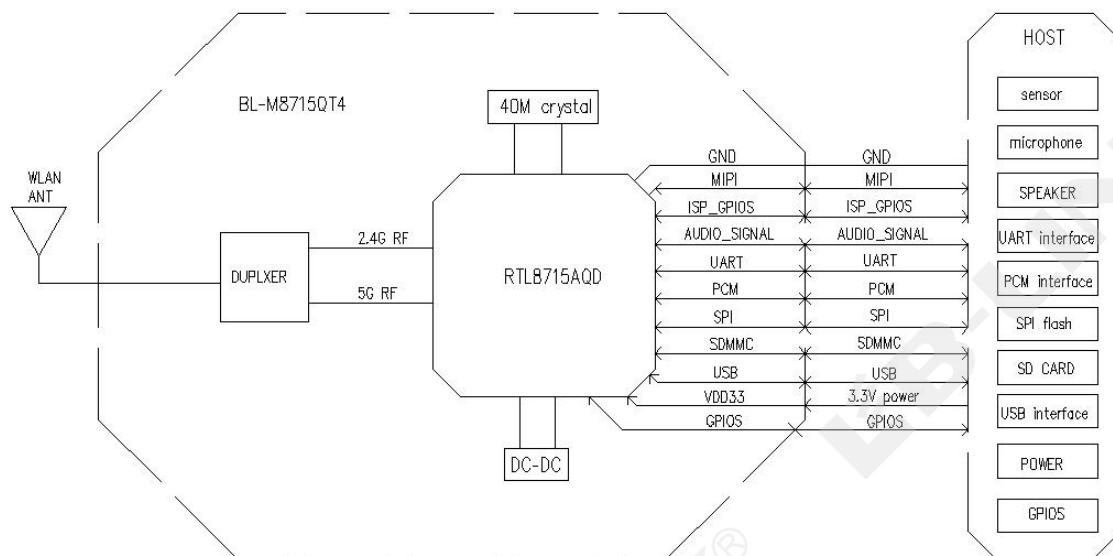
(Top View)



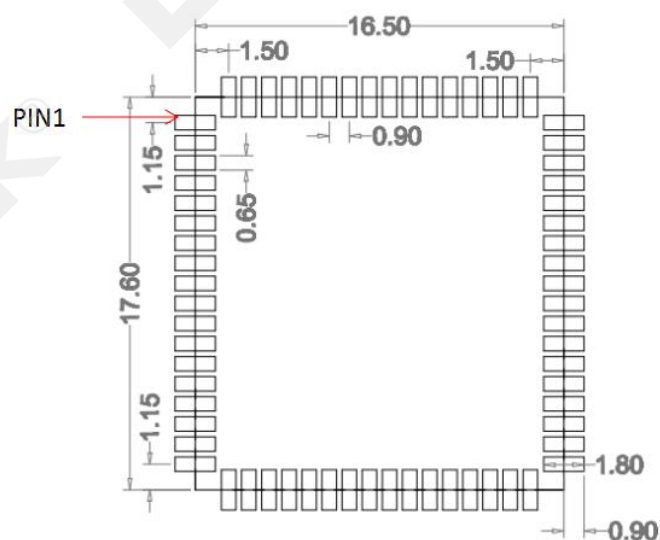
(Bottom View)

## 6. Application Information

### 6.1 Typical Application Circuit

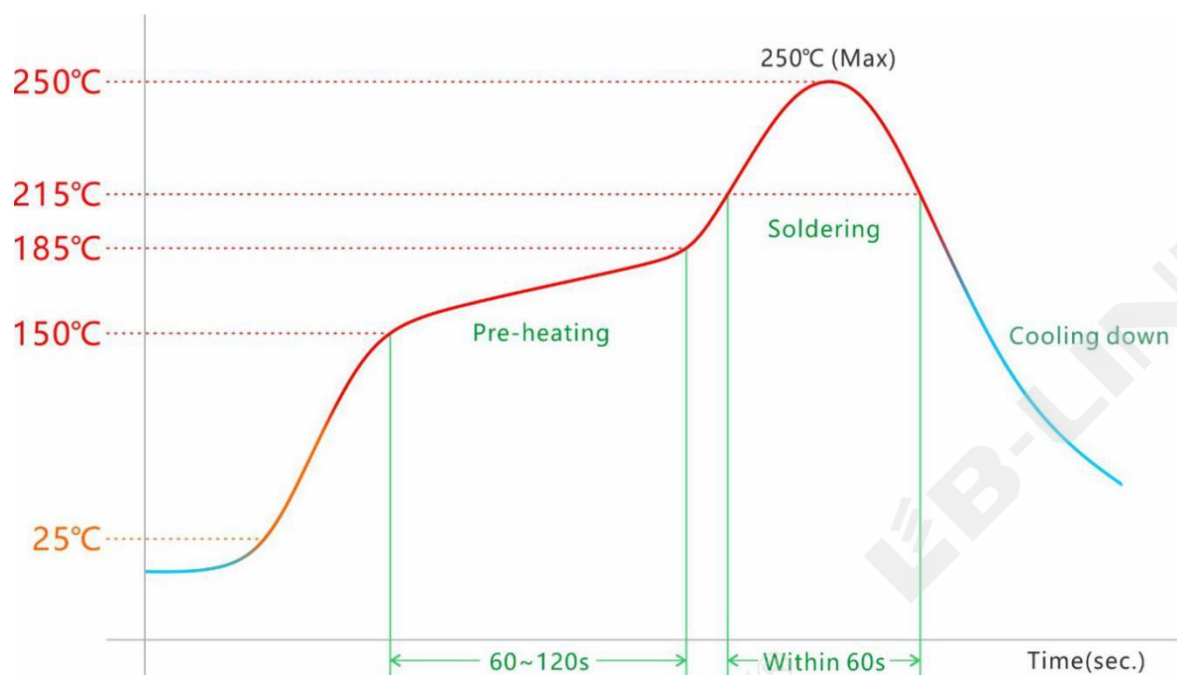


### 6.2 Recommend PCB Layout Footprint



(Top View)

### 6.3 Reflow Soldering Standard Conditions



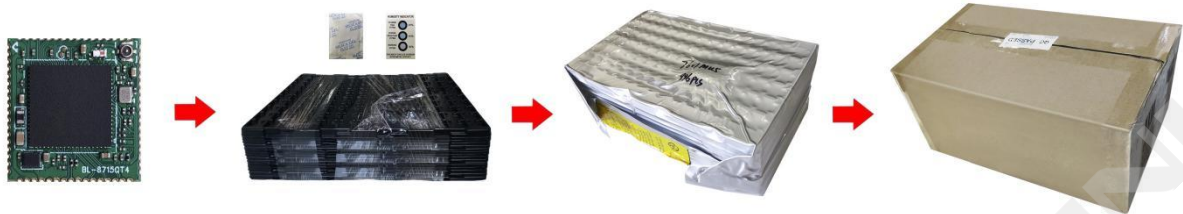
Please use the reflow within 2 times.  
Set up the highest temperature within 250°C.

## 7. Key Components Of Module

| No. | Parts   | Specification        | Manufacturer                             | Note |
|-----|---------|----------------------|------------------------------------------|------|
| 1   | Chipset | RTL8715AQD-VR3-CG    | Realtek                                  |      |
| 2   | PCB     | BL-M8715QT4          | Shen Zhen Tie Fa Technology              |      |
|     |         |                      | Guang Dong KINGSHINE ELECTRONICS CO.,LTD |      |
|     |         |                      | Quzhou Sunlord Electronics Co., Ltd      |      |
| 3   | Crystal | 40MHZ-10PPM-9pF-2016 | ASLT ELECTRONICS TECHNOLOGY CO.,LTD.     |      |
|     |         |                      | LUCKI CM ELECTRONICS CO,LTD              |      |
|     |         |                      | SHENZHEN KAIYUEXIANG ELECTRONICS CO,LTD  |      |

## 8. Package and Storage Information

### 8.1 Package Dimensions



Package specification:

1. 100 modules per blister plate and 2,500 modules per box.
2. The blister is bound with wire membrane and put into anti-static vacuum bag.
3. Put 1 bag of dry beads (20g) in each anti-static vacuum bag. 1 pcs 3 point humidity card.
4. The outer box size is 35.2\*21.5\*15.5cm.

### 8.2 Storage Conditions

Absolute Maximum Ratings:

Storage temperature: -40°C to +85°C

Storage humidity: 10% to 95% RH (Non-Condensing)

Recommended Storage Conditions:

Storage temperature: 5°C to +40°C

Storage humidity: 20% to 90% RH

Please use this Module within 12month after vacuum-packaged.

The Module shall be stored without opening the packing.

After the packing opened, the Module shall be used within 72hours.

When the color of the humidity indicator in the packing changed, the Module shall be baked before soldering.

Baking condition: 60°C, 24hours, 1time.

ESD Sensitivity:

ESD Protection: 4KV(HBM ,Maximum rating)

The Module is a static-sensitive electronic device.

Do not operate or store near strong electrostatic fields.

Take proper ESD precautions!



**ESD CAUTION**